CTμL9952

DUAL 2-INPUT NOR GATE

COMPLEMENTARY TRANSISTOR MICROLOGIC® INTEGRATED CIRCUITS

+15°C TO +55°C TEMPERATURE RANGE

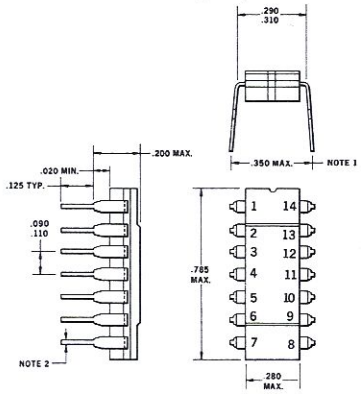
GENERAL DESCRIPTION–The CTμL 9952 Dual 2-Input Inverter Gate provides logic gating at its input and output terminals. Compatible with all other CTμL elements, the output can be tied to any other element to perform the wired OR function.

The 9952 may be used to set and restore the system logic levels; having a high noise immunity, it can drive and be driven by a number of cascaded CTμL AND-OR gates. The following data, stressing worst case conditions, plus 100% testing by Fairchild Semiconductor, will assure the designer of proper worst case performance in his own system.

The CTμL 9952 is designed for general purpose industrial and commercial usage where high speed logic is required. It is packaged in the versatile Dual-In-Line* package, which is a hermetically sealed ceramic package intended for low-cost insertion techniques.

TYPICAL DUAL IN-LINE* PACKAGE

in accord with JEDEC (TO-116) outline

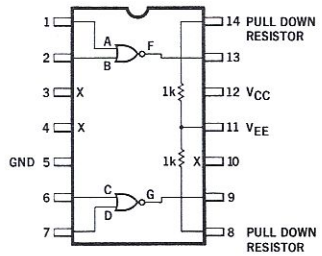


NOTES:

1. Leads are intended for insertion in hole rows on .300" centers. They are purposely shipped with "positive" (.350) misalignment to facilitate insertion.
2. Board-drilling dimensions should equal your practice for a conventional .020 inch diameter lead.

CONNECTION DIAGRAM

TOP VIEW



POSITIVE LOGIC $F = \overline{A+B}$
$G = \overline{C+D}$

NOTE: X = NOT CONNECTED

FEATURES

- **POWER SUPPLIES ARE +4.5 V ±10% AND —2.0 V ± 10%**
- **HIGH FAN-OUT CAPABILITY — 12**
- **TEMPERATURE RANGE — +15°C TO +55°C**
- **OPTIONAL PULLDOWN 1.0 k RESISTOR FOR OPTIMUM SPEED**
- **LOW POWER DISSIPATION**
- **LOW PROPAGATION DELAY — 7.0 ns TYPICAL**
- **LOGIC SWING OF 3.0 V**
- **HIGH NOISE IMMUNITY > 1.0 V AT FAN-OUT = 12**

PURCHASING INFORMATION

Use the ten-letter code U6A995279X for ordering purposes.

All units are marked CTμL-995279 and date code unless otherwise specified.

*Fairchild Patent Pending

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

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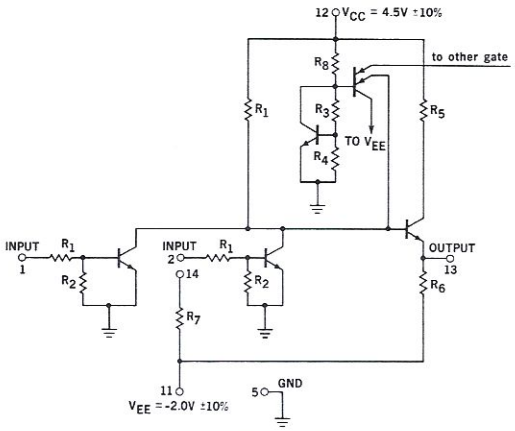
MANUFACTURED UNDER ONE OR MORE OF THE FOLLOWING U. S. PATENTS: 2981877, 3015048, 3025589, 3064167, 3108359, 3117260; OTHER PATENTS PENDING.

CTμL-9952 COMPLEMENTARY TRANSISTOR MICROLOGIC® IC

SCHEMATIC DIAGRAM



NOTE: Only one 2-input inverter gate shown.

ABSOLUTE MAXIMUM RATINGS

(above which the useful life may be impaired)

Maximum Current in or out of a pin	100 mA
Maximum Chip Temperature	+150°C
Maximum Power Dissipation	1.0 Watt
Maximum Voltage Applied to any Input Pin	10 Volts
Maximum Negative Voltage Applied to any Input Pin	−4.0 Volts
Maximum Voltage Applied to Output Pin	6.0 Volts

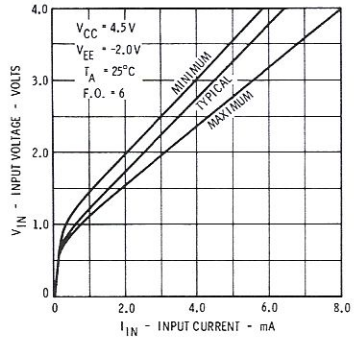
DC TESTS

TEST (at T_A = 25°C)	LIMITS				CONDITIONS			
	MIN.	TYP.	MAX.(1)	UNITS	V_{CC}	V_{EE}	LOAD TO V_{EE}	COMMENTS
Output ONE Level	2.35	2.50		Volts	4.05 V	−2.20 V	F.O.(2) = 12	Inputs to +0.8 V sequentially. Guarantees input low threshold >0.80 V; and output ONE level >2.35 V.
Output ZERO Level		−0.50	−0.36	Volt	4.95 V	−1.80 V	F.O. = 1	Inputs to 1.25 V sequentially. Guarantees input high threshold <1.25 V; output ZERO level <−0.36 V.
Output ONE Level		2.75	2.90	Volts	4.95 V	−1.80 V	F.O. = 1	Inputs to −0.70 V simultaneously. Guarantees output never more positive than 2.90 V.
Input Current	4.20	5.30	6.86	mA	4.05 V	−1.80 V	No load	Inputs to 3.5 V simultaneously. Guarantees input loading <1.5 AND gate loads.
Output Resistor	1.6 k	2.0 k	2.4 k	Ohms	4.05 V	−2.20 V	No load	Inputs to −0.7 V simultaneously. (Outputs to 3.5 V sequentially.) Guarantees output OR tie <1.0 AND-OR gate loads.
Input Pulldown Resistor	0.8 k	1.0 k	1.2 k	Ohms	4.05 V	−2.20 V	No load	Resistor to 3.50 V sequentially. Guarantees 1 k resistor available for input pulldown is within 20% of nominal value.
Output Falling Delay, t_{df}		6	12	ns	4.50 V	−2.00 V	F.O. = 12	See t_{PD} Test Circuit
Output Rising Delay, t_{dr}		8	14	ns	4.50 V	−2.00 V	F.O. = 12	See t_{PD} Test Circuit
Positive Supply Current	18.5	30	36.2	mA	4.95 V	−2.20 V	No load	Inputs to +3.50 V simultaneously. Tests internal resistors to be no more than ±20% from nominal.
Negative Supply Current	6.75	8	14.8	mA	4.95 V	−2.20 V	No load	Inputs to −0.70 V simultaneously. Test internal resistors to be no more than ±20% from nominal.

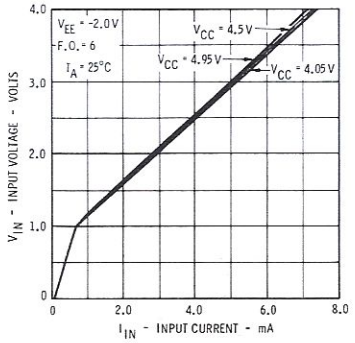
NOTES: (1) "Maximum" means "no more positive than"
(2) F.O. = Fan-Out: F.O. = 12 equivalent to 133 Ω to −2.20 V under worst case conditions.
F.O. = 1 equivalent to 2.4 kΩ to −1.80 V under worst case conditions.

INPUT CHARACTERISTICS

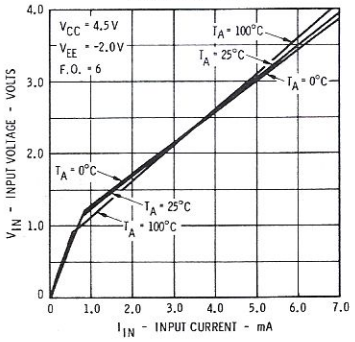
TOLERANCE VARIATION OF PARAMETERS



AS A FUNCTION OF COLLECTOR SUPPLY VOLTAGE

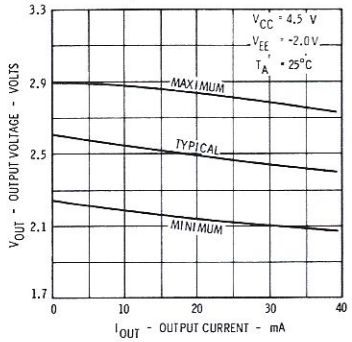


AS A FUNCTION OF TEMPERATURE

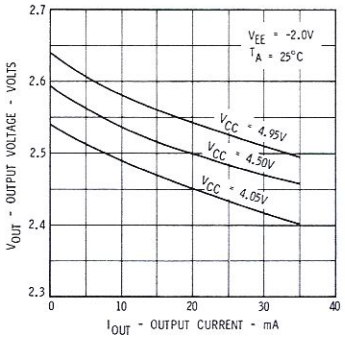


OUTPUT CHARACTERISTICS

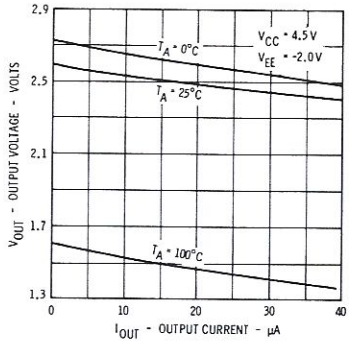
TOLERANCE VARIATION OF PARAMETERS



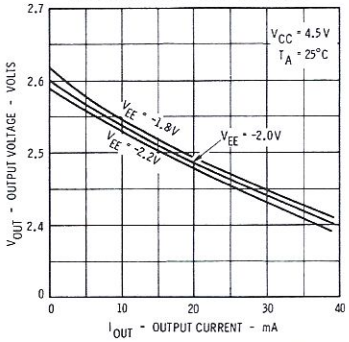
AS A FUNCTION OF COLLECTOR SUPPLY VOLTAGE



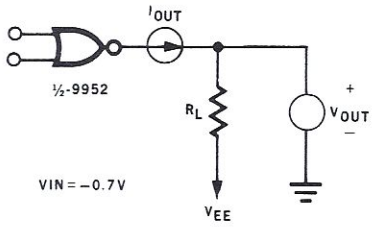
AS A FUNCTION OF TEMPERATURE



AS A FUNCTION OF NEGATIVE SUPPLY VOLTAGE

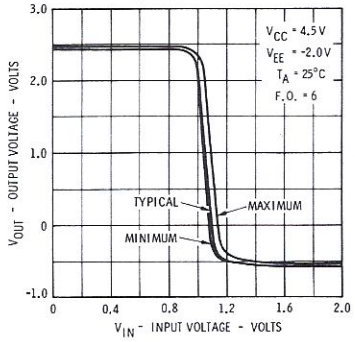


SCHEMATIC DIAGRAM

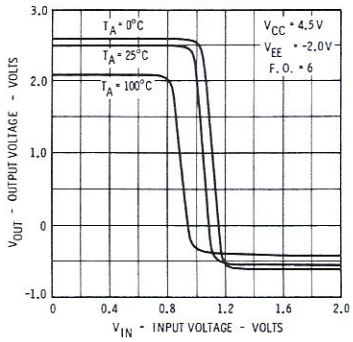


TRANSFER CHARACTERISTICS

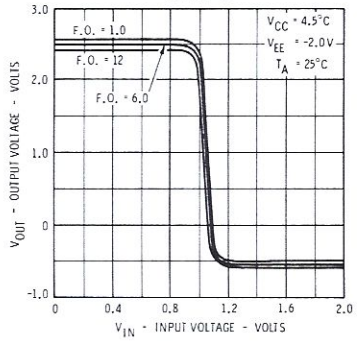
TOLERANCE VARIATION OF PARAMETERS



AS A FUNCTION OF TEMPERATURE

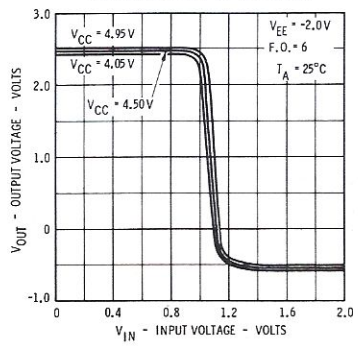


AS A FUNCTION OF FAN-OUT

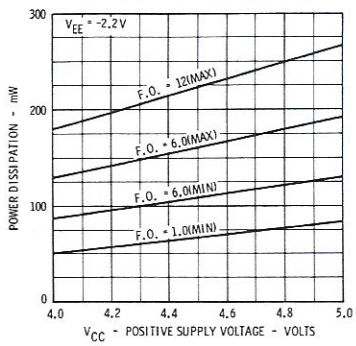


NOTE: Variation of V_{EE} does not alter transfer characteristics.

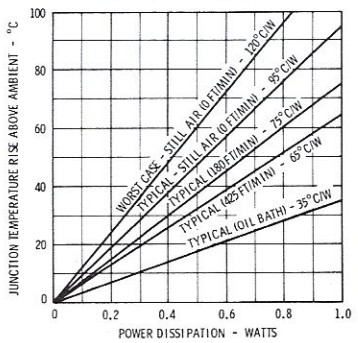
AS A FUNCTION OF POSITIVE SUPPLY VOLTAGE



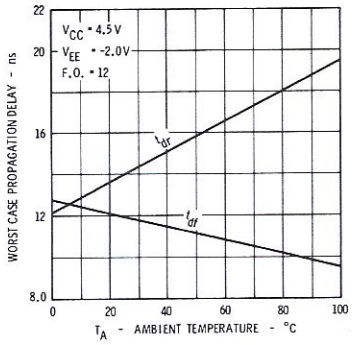
POWER DISSIPATION VERSUS POSITIVE SUPPLY VOLTAGE



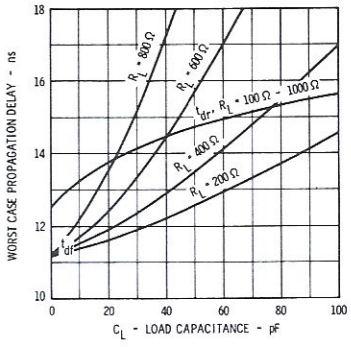
WORST CASE JUNCTION TEMPERATURE VERSUS POWER DISSIPATION


WORST CASE - STILL AIR (0 FT/MIN) - 120°C/W
TYPICAL - STILL AIR (0 FT/MIN) - 85°C/W
TYPICAL (180 FT/MIN) - 75°C/W
TYPICAL (425 FT/MIN) - 65°C/W
TYPICAL (OIL BATH) - 35°C/W
JUNCTION TEMPERATURE RISE ABOVE AMBIENT - °C
POWER DISSIPATION - WATTS

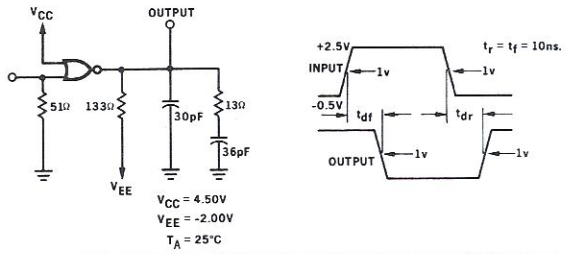
WORST CASE PROPAGATION DELAY VERSUS AMBIENT TEMPERATURE



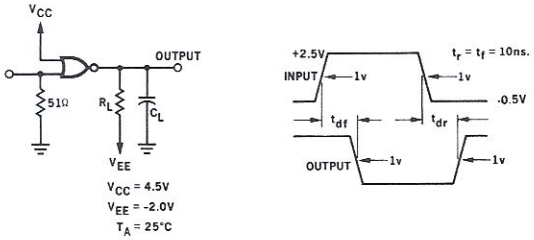
WORST CASE PROPAGATION DELAY VERSUS LOAD CAPACITANCE AS A FUNCTION OF LOAD RESISTANCE



t_{PD} TEST CIRCUIT



t_{PD} TEST CIRCUIT FOR ABOVE



APPLICATION INFORMATION

The electrical specification tests performed under the conditions set, emphasize the worst case results and should be considered as conservative limits. Throughout this data sheet, WORST CASE should be interpreted as using power supplies, internal resistors, transistor parameters and external loads having extreme loads chosen in a manner to guarantee proper operation under worst case conditions.

LOADING RULES: Each input to the CTμL 9952 represents 1.5 unit loads.
(One unit load is defined as an input to the CTμL AND-OR gate.)

a) Connecting the 1.0 kΩ pulldown resistor to the input adds two unit loads to the fan-in.

b) Connecting the 1.0 kΩ pulldown resistor to the output reduces the fan-out by two unit loads.

c) Each wired-OR connection reduces the fan-out by one.

PULLDOWN RESISTOR: Two pulldown 1.0 kΩ resistors are built into the package with one end tied to the negative power supply (V_{EE}). Connecting the 1.0 kΩ resistor to the CTμL 9952 input will improve the turn-off characteristics and speed up the output rising propagation delay. When the input of the CTμL 9952 is driven by four or more AND-OR gates, there is no advantage in connecting the 1.0 kΩ resistor to the same input. The pulldown resistor may also be connected to the CTμL 9952 output. This will improve the output falling propagation delay when low fan-out is used.

WIRED OR: A powerful feature of the CTμL 9952 inverter is that the output may be tied together with the output of any other element in the CTμL family to form the positive OR function at the tie point, thus achieving two logic functions without additional propagation delay.

INTERFACING: The CTμL 9952 inverter gate serves as an excellent interfacing link between external signals coming from other logic forms or peripheral equipment and the CTμL family.

NOISE IMMUNITY: The CTμL 9952, having excellent noise immunity under maximum loading and worst case conditions, is used primarily to restore logic levels degraded after passing through several CTμL AND-OR gates.

HIGH SPEED CONSIDERATIONS: The high-speed logic operation available using CTμL requires that care be exercised in packaging and interconnection techniques. Normally logic circuits using emitter followers as drivers have a tendency to oscillate when driven by high-speed pulse signals. Each CTμL 9952 includes a clamping network so designed that it reduces ringing at high-speed operation. These features eliminate the necessity for the use of strip lines or coaxial cables for all but the longest lines. However, care must still be exercised in the layout of printed circuit boards. Any one line over 12″ in length tied to a gate output should be terminated in a 200 Ω resistor to ground. Such a 200 Ω resistor approximates the characteristic impedance of the back panel wiring and is considered equivalent to a fan-out of 4.

SHORT CIRCUIT PROTECTION: The CTμL 9952 inverter gate output is protected by a limiting resistor at the output and may sustain prolonged short circuit to ground with V_{CC} not greater than 5.0 V. Excessive destructive heat may develop when more than one output in a single package is short circuited to ground. In general, short circuiting the output should be avoided.

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